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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,541	02/10/2004	Amir Morad	13757US03	3126

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2483	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,541	MORAD ET AL.	
	Examiner	Art Unit	
	Tung Vo	2483	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 10 October 2010.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 10-36 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 10-36 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02/10/2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 10-20 and 24-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph et al. (US 5,825,430) in view of Hinchley et al (US 6,490,250) as set forth in the previous office action mailed on 06/10/10.

3. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph et al. (US 5,825,430) in view of Hinchley et al (US 6,490,250) in view of Ishihara et al. (US 6,516,031) as set forth in the previous office action mailed on 06/10/10.

4. Claims 23 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph et al. (US 5,825,430) in view of Hinchley et al (US 6,490,250) and Ishihara et al. (US 6,516,031), and further in view of Kopet et al. (US 5,448,310) as set forth in the previous office action mailed on 06/10/10.

5. Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430) as set forth in the previous office action mailed on 06/10/10.

6. Claims 13 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430), and further in view of Bruck (US 6,519,289) as set forth in the previous office action mailed on 06/10/10.

7. Claims 14, 17-19, 27, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430) in view of Hinchley et al. (US 6,490,250) as set forth in the previous office action mailed on 06/10/10.

8. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430), and further in view of Boice et al. (US 6,823,013) as set forth in the previous office action mailed on 06/10/10.

9. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430) and Boice et al. (US 6,823,013), and further in view of Kopet et al. (US 5,448,310) as set forth in the previous office action mailed on 06/10/10.

Response to Arguments

10. Applicant's arguments filed 10/10/2010 have been fully considered but they are not persuasive.

The applicant noted that the Bruck (US 6,519,289) is not on any PTO-892 form in the remarks. The Bruck (US 6,519,289) is now in PTO-892 form of record.

I. The combination of Adolph and Hinchley

The applicant argues that the Office inconsistent in its identification of the aspect of Adolph that teaches the applicants' claimed invention as "first multiplexed stream". The applicant further argues that "MUX1" of Adolph produces "first multiplexed stream" and "MMUX" that also produces "first multiplexed stream".

It is noted that the applicants claim "**multiplexer circuitry** that operates in **a first mode** and **a second mode**, which when operating in **the first mode** produces **a first multiplexed stream** from **first compressed video**, **first compressed audio**, **second compressed video**, and **second compressed audio**; and which when operating in **the second mode** concurrently produces **the first multiplexed stream** from **the first compressed video** and **the first compressed audio**, and produces **a second multiplexed stream** from **the second compressed video** and the **second compressed audio.**"

The applicant admitted in the remarks page 17 that Applicants' claimed "first mode" and "second mode" characterize operation of Applicants' claimed "multiplexer circuitry," in which in the claimed "first mode," the "multiplexer circuitry" produces a "first multiplexed stream" using four components, namely, "first compressed video," "first compressed audio," "second

compressed video," and second compressed audio." In the claimed "second mode," however, the claimed "multiplexer circuitry" produces the "first video stream" using the two components "first compressed video" and "second compressed video," and produces, in addition, a "second multiplexed stream" using the two components "second compressed video" and "second compressed audio." Thus, the "first mode" and "second mode" define the video and audio content of the "first multiplexed stream" and the "second multiplexed stream."

The examiner respectfully disagrees with the applicant. It is submitted that Adolph clearly teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3).

MODES	ADOLPH TEACHES
IN THE FIRST MODE: **multiplexer circuitry** that operates when operating in **the first mode** produces **a first multiplexed stream** from **first compressed video**, **first compressed audio**, **second compressed video**, and **second compressed audio**	MMUX OF FIG. 3 using four components as VE1, AE1, VE2, and AE2 of fig. 3
IN THE SECOND MODE: concurrently produces **the first multiplexed stream** from **the first compressed video** and **the first compressed audio**	MUX1 OF FIG. 3 using two components as VE1 and AE1 of fig. 3
IN THE SECOND MODE: produces **a second multiplexed stream** from **the second compressed video** and the **second compressed audio**	MUX 2 OF FIG. 3 using two components as VE2 and AE2 of fig. 3

It is noted that the applicant further argues that "MUX1" of Adolph produces "first multiplexed stream" and “MMUX" that also produces "first multiplexed stream”. However, the applicant fails to show which "first multiplex stream" is produced in the first mode and which "first multiplexed stream" is produced in the second mode. As mentioned above, the claimed invention clearly states a first multiplexed stream is produced in the first mode and the first

multiplexed is produced in the second mode concurrent with a second multiplexed stream. Adolph clearly teaches MMUX of fig. 3 produces a first multiplexed stream in the first mode, and MUX1 of fig. 3 concurrently produces the first multiplexed stream and MUX 3 of fig. 3 produces a second multiplexed stream in the second mode.

The applicant further argues that Adolph does not disclose transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and transmits the second multiplexed stream to circuitry external to the device via a second output of the device.

The examiner strongly disagrees with the applicant. It is submitted that Adolph teaches the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio in the first mode or the first compressed video and first compressed audio in the second mode, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

The applicant repeatedly argues that Hinchley does not disclose any text to describe the claimed as specified in claim 10, and "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder".

The examiner respectfully disagrees with the applicant. It is submitted that the multiplexer circuitry of the present invention is disclosed in the specification in figure 5 as follows:

[0040] According to an embodiment of the present invention, device 100 is a parallel digital processor implemented on a single chip and designed for the purposes of real-time video/audio compression and multiplexing, MPEG-1 and MPEG-2 encoding.

[0061] Bitstream processor 112 encodes the compressed video data into a standard MPEG-1 and MPEG-2 format, in accordance with a sequence known in the art of encoding commands. Bitstream processor 112 transfers compressed video data streams to multiplexing processor 114.

[0063] Multiplexing processor 114 multiplexes the compressed video and the compressed audio and/or user data streams (as received from bitstream processor 112 and audio encoder 113) and generates, according to a sequence of optimized multiplexing commands, MPEG-2 standard format streams such as packetized elementary stream, program stream, transport stream and the like. Multiplexing processor 114 transfers the multiplexed video/audio/data streams to a compressed data stream output and to memory controller 110. Multiplexing processor 114 outputs a stream of compressed video and/or audio and/or data.

[0064] Global controller 104 controls and schedules the video input buffer 102, the motion estimation processors 105 and 106, the digital signal processor 108, the memory controller 110, the bitstream processor 112, the 12C/GPIO interface, and the multiplexing processor 114. Global controller 104 is a central control unit that synchronizes and controls all of

the internal chip units and communicates with all of the internal chip units using data-instruction-device buses.

The disclosure above encompass the claimed features as “multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio”.

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Let compare the multiplexing circuit of Hinchley and the present invention as follows:

<table>
<tr><th>Hinchely</th><th>The present invention</th></tr>
<tr><td>

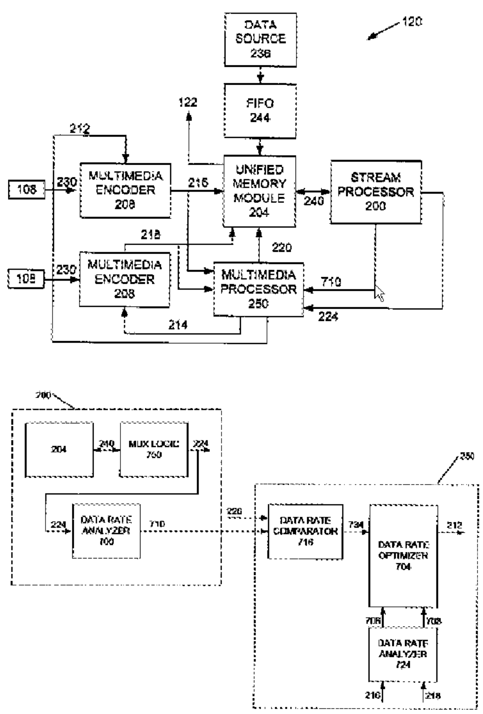
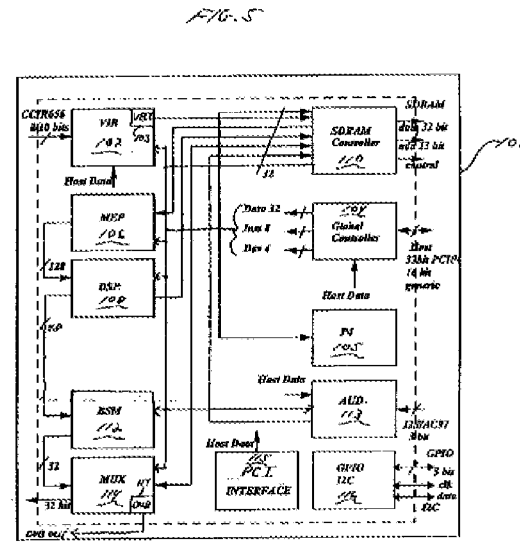


FIGURE 7

</td><td>



</td></tr>
<tr><td>FIG. 7 is a more detailed block diagram of an embodiment of the stream processor 200 and multimedia processor 250 in accordance with the present invention. The stream processor 200 includes MUX logic 750 which performs conventional multiplexing operations in accordance with recognized standards such as MPEG2 to generate the combined multimedia stream 224. Combined multimedia stream 224 is preferably a program or transport stream as specified in MPEG2. The MUX logic 750 accesses the unified memory module 204 through data line 240 to retrieve the data and the instructions to perform on the data. After performing the required operations, the data 224 is temporarily written back to memory 204, for later transfer to the communications device 112 or other recipient of the Program or Transport Stream 224.</td><td>[0063] Multiplexing processor 114 multiplexes the compressed video and the compressed audio and/or user data streams (as received from bitstream processor 112 and audio encoder 113) and generates, according to a sequence of optimized multiplexing commands, MPEG-2 standard format streams such as packetized elementary stream, program stream, transport stream and the like. Multiplexing processor 114 transfers the multiplexed video/audio/data streams to a compressed data stream output and to memory controller 110. Multiplexing processor 114 outputs a stream of compressed video and/or audio and/or data.

This disclosure encompasses the claimed features</td></tr>
</table>

Based upon the comparison above, Hinchley's MUX logic (750 of fig. 7) has the same functions (MPEG2 standards) as Multiplexing processor (114 of fig. 5) of the present invention. Therefore, Hinchley teaches the claimed features.

Hinchley further teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention. Therefore, the functions of MPEG-2 encoders (208 of fig. 2) of Hinchley meet the claimed features. Hinchley further teaches the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53). In view of the discussion above, the claimed invention is unpatentable over Adolph and Hinchley.

II. The combination of Adolph, Hinchley, and Ishihara.

The applicant argues that Adolph and Hinchley does not teach the features as specified in claims 10 and 24, therefore claims 21, 22, 34, and 35 are not taught by the combination of Adolph, Hinchley, and Ishihara.

The examiner strongly disagrees with the applicant. It is submitted that Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first

compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second

compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Hinchley further teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention; and the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53).

Ishihara teaches a plurality of search processors (7 of fig. 2) for performing motion analysis in parallel, each upon a different portion of a macroblock (PE1, PE2….PE33 of fig. 7; e.g. fig. 13). Therefore, one of ordinary skill in the art would have been obvious to modify the processor array (7 of fig. 2) of Ishihara into the motion estimation of the combination of Adolph and Hinchley to provide an improvement for reducing a hardware volume.

III. The combination of Adolph, Hinchley, Ishihara, and Kopet.

The applicant argues that Adolph and Hinchley does not teach the features as specified in claims 10 and 24, therefore claims 23 and 36 are not taught by the combination of Adolph, Hinchley, and Ishihara.

The examiner strongly disagrees with the applicant. It is submitted that Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

Hinchley discloses multiplexer circuitry (200 of fig. 2, note the stream processor, 200 of fig. 2, comprises the MUX LOGIC (750 of fig. 7) is compliant with MPEG2 standard, which has the same functions as multiplexing circuitry as disclosed above of the present invention) that

operates in a first mode and a second mode (MUX logic (750 of fig. 7) performs multiplexing operations that encompass a first mode and second mode). Since Hinchley discloses the MUX logic (750 of fig. 7) have multiplexing operations as modes with recognized standards such as MPEG2, col. 6, lines 12-26, so the MUX logic performs when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio, which is the same the multiplexing circuitry, 114 of fig. 5, of the present invention as disclosed in the specification, [0040], [0061], [0063], and [0064].

Hinchley further teaches encoders (208 of fig. 2, col. 3, lines 34-38) that are compliant with MPEG-2 compression standards (col. 3, lines 30-33), wherein claimed first and second encoders are also compliant with MPEG-2 compression standard. Since the both Hinchley uses the MPEG-2 encoders (208 of fig. 2), the disclosure of MPEG-2 encoders of Hinchley performs the same functions as the first and second MPEG-2 encoders of the claimed invention; and the multimedia engine as control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (col. 4, lines 49-53).

Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29). Therefore, it would have been obvious to one of ordinary skill in the art to

modify the teachings of Kopet into the combined motion estimation of Adolph, Hinchley, and Ishihara in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

IV The combination of Krishnamurthy and Adolph.

The applicant argues that the Office Action has not identify the required elements or suggestion or motivation to arrive at the required elements in the prior art sufficient to support such a purported rationale, pages 11-13 of the appeal brief.

The examiner respectfully disagrees with the applicant. It is submitted that Krishnamurthy teaches a single-chip audio/video encoder device (fig. 3) that comprises first encoder circuitry (306, ENC1 of fig. 3), second encoder circuitry (306, ENCn of fig. 3), multiplexer circuitry (308 of fig. 3), controller circuitry (304 of fig. 3), and at least one bus interface (302 of fig. 3); wherein the first encoder circuitry (306, ENC1 of fig. 3) comprises: a first video encoder (302 of fig. 3), a first audio encoder (322 of fig. 3), a first motion estimation processor (MPEG-2 encoder, 320 of fig. 2, would obviously comprise a motion estimation processor); wherein the second encoder circuitry (306, ENCn of fig. 3) comprises: a second video encoder (320 of fig. 3), a second motion estimation processor (320 of fig. 3, ENCn, MPEG-2 encoder obviously comprise a motion estimation processor), a second audio encoder (322, ENCn of fig. 3); wherein the multiplexer circuitry (308 of fig. 3) multiplexes the compressed video and audio outputs from the encoders (306 of fig. 3) to produce the multiplexed signal, and the multiplexed signal is transmitted to circuitry external to the device (col. 19, lines 50-52, note the circuitry would obviously be a serial output port).

Krishnamurthy suggests models of encoders and multiplexer (fig. 3) will be useful for the advance allocation statistical multiplexer (e.g. 308 of fig. 3) that have mostly been developed for natural video and need modifications for game and web content. This is evidence to one skill in the art to use any suitable and conventional device to modify the statistical multiplexer (col. 15, lines 45-50).

Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed

audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

Since Krishnamurthy and Adolph teach the video and audio signals accordance to MPEG standard and suggest modifications that would be made; therefore one skill of ordinary in the art would combined the suggested teachings of Krishnamurthy and Adolph to make obvious claimed invention.

Note not only the specific teachings of a reference but also reasonable inferences which the artisan would have logically drawn therefrom may be properly evaluated in formulating a rejection. In re Preda, 401 F.2d 825, 159 USPQ 342 (CCPA 1968) and In re Shepard, 319 F.2d 194, 138 USPQ 148 (CCPA 1963). Skill in the art is presumed. In re Sovish, 769 F.2d 738, 226 USPQ 771 (Fed. Cir. 1985). Furthermore, artisans must be presumed to know something about the art apart from what the references disclose. In re Jacoby, 309 F.2d 513, 135 USPQ 317 (CCPA 1962).

The obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969)). Every reference relies to some extent on knowledge of persons skilled in the art to complement that which is disclosed therein. In re Bode, 550 F.2d 656, 193 USPQ 12 (CCPA 1977).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Office Action above, paragraph 9, suggests all limitations to make obvious the claimed invention.

The applicant argues that the cited portion of Krishnamurthy in the Office Action does not teach " wherein the multiplexer circuitry operates in a first mode that multiplexes the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio to produce a first multiplexed stream coupled, and operates in a second mode that multiplexes the first compressed video and the first compressed audio to produce the first multiplexed stream and multiplexes the second compressed video and the second compressed audio to produce a second multiplexed stream".

The examiner respectfully disagrees with the applicant. It is submitted that the multiplexer circuitry *(308 of fig. 3, note the stat-mux board can receive up to 24 different channels of transport bit-streams, col. 18, lines 50-52, from 24 encoders,306-306N of fig. 3, N=24, col. 18, line 15)*operates in a first mode *(col. 20, lines 22-26, "a multi-channel mode" would obviously be considered as a first mode, and the first mode is controlled by the overall board-level controls, col. 19, lines 39-42)* that multiplexes the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio to produce a first multiplexed stream *(Note the stat-mux, 308 of fig. 3, multiplexes up to 24 different channels of the transport bitstreams from 24 encoders, therefore the stat-mux would encompass to multiplex the first compressed video, the first compressed audio, the second compressed video, and the second compressed audio as four different channels of transports of bitstreams.* and operates in a mode that multiplexes the first compressed video and the first compressed audio to

produce the first multiplexed stream *(326 of fig. 3, to multiplex the first compressed video and the first compressed audio to produce the first multiplexed stream)* and multiplexes the second compressed video and the second compressed audio to produce a second multiplexed stream coupled via a second output (*326 of fig. 3, to multiplex the second compressed video and the second compressed audio to produce the first multiplexed stream; col. 19, lines 42-45, 328 of fig. 3, SSI of fig. 3).*

The applicant argues that Adolph does not teach the claimed features as specified in claim 10.

The examiner strongly disagrees with the applicant. It is submitted that Adolph teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in **the first mode** (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in **the second mode** (MUX1 of fig. 3) concurrently produces **the first multiplexed stream** (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3), the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream)

comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3. In view of the discussion above, the claimed invention is unpatentable over the combination of Krishnamurthy and Adolph.

The applicant further argues that the cited figure 3 of Krishnamurthy does not teach circuitry external to the device.

The examiner respectfully disagrees with the applicant. It is submitted that Krishnamurthy teaches the outputs from the stat-mux are transmitted to circuitry *(col.19, lines 50-52, note the on-chip DMA will automatically move data from the TS output buffer of on-chip memory to the serial output port, this is evidence that the multiplexed compressed bitstreams are transmitted to the serial output port as circuitry)* external to the device (306 and 308 of fig. 3). It is noted that the circuitry external to the device is well known in the art and is taught by Hinchley *(Note the circuitry external (116 or 112 of fig. 1) to the device (120 of fig. 1, see also fig. 2)*.

The applicant further argues that Krishnamurthy does not teach "a first output to circuitry external to the device", and "a second output to circuitry external to the device".

The examiner respectfully disagrees with the applicant. It is submitted that Krishnamurthy teaches the multiplexer, 308 of fig. 3, for outputting the multiplexed bitstream to circuitry external to the device by the output port (342 of fig. 3); this indicates that the output of the multiplexed bitstream must be transmitted to circuitry external to the device such as a

memory device or a communication device. It is noted that circuitry external from the single chip audio/video encoder device is well known in the art and is taught by Hinchley (figure 1, circuitry as 112 and 116, external to the device as 120).

The applicant further argues that Krishnamurthy does not teach, suggest, or render obvious controller circuitry that synchronizes operation of the first encoder, the second encoder and the multiplexer circuit.

The examiner respectfully disagrees with the applicant. It is submitted that Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, harmonize, or orchestrate operation of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuit properly working.

Krishnamurthy further discloses Computer systems in accordance with the present invention avoid PCI bus delay by using the built-in multi-channel Synchronized Serial Interface (SSI) ports of multiple Digital Signal Processors (DSPs), where each DSP performs video and audio encoder control, PES/TS layer multiplexing, and computation of statistical measurements of its corresponding video stream payload. The DSPs' on-chip memories may also eliminate the need for bitstream First-In, First-Out (FIFO) chips and some common SDRAM (Synchronized Dynamic Random Access Memory) chips (col. 17, line 65-col. 18, line 8). There is CPLD (Complex Programmable Logic Device) or FPGA (Field-Programmable Gate Array) based deframing firmware to split the video and audio data, and to reproduce the video synchronization signals for the MPEG2 video encoder chip (col. 19, lines 18-22), the above disclosure is

evidence that the Krishnamurthy's controller circuitry synchronizes operation of the first encoder, the second encoder and the multiplexer circuit.

V. The combination of Krishnamurthy, Adolph, and Bruck.

The applicant argues that the combination of Krishnamurthy, Adolph, and Bruck doses teach the claimed features as specified in claims 13 and 26.

The examiner strongly disagrees with the applicant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above.

Bruck teaches wherein the video encoder performs luminance and chrominance filtering (col. 1, lines 59-col. 2, line 8). Krishnamurthy teaches the encoder (306 of fig. 3) for encoding video and audio stream based on the MPEG-2 standards, wherein the MPEG-2 standard would obviously have the luminance and chrominance for filtering by Bruck (col. 1, lines 59-col. 2, line 8). Taking the teachings of Krishnamurthy, Adolph, and Bruck as a whole, it would have been obvious to one of ordinary skill in the art to modify the luminance and chrominance filtering of Bruck into Krishnamurthy and Adolph to improve the picture quality.

VI. The combination of Krishnamurthy, Adolph, and Hinchley.

The applicant argues that the combination of Krishnamurthy, Adolph, and Hinchley doses teach the claimed features as specified in claims 14, 17-19, 27, 30-32.

The examiner respectfully disagrees with the applicant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above. Krishnamurthy further teaches wherein the at least one bus interface (PCI BUS, 302 of fig. 3)

enables transfer of one or both of uncompressed audio data and/or video data for processing by the device (318 of fig. 3); wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one bus interface ("C" programmable language and micro-codes are used to instruct elements in figure 3; col.18, lines 28-33; col. 19, lines 26-28).

Hinchley teaches a first storage external to the device and a second storage external (108 and 116 of fig. 1) to the device (120 of figs. 1 and 2) and the at least one bus interface is configurable to act as a bus master (122 of fig. 1) using direct memory access (Note the bus (122) would obviously be the PCI bus and/or direct memory access, which serves the same purpose of transferring and receiving data to and from components within the circuit (100 of fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the first and second storages and random access memory with the interface bus (108, 116, and 122 of fig. 1) of Hinchley into the first and second interface (318 of fig. 2) Krishnamurthy and Adolph to provide an integrated multimedia encoding system which operates with reduced memory storage requirements is also needed. In view of the discussion above, the claimed invention is unpatentable over the combination of Krishnamurthy, Adolph, and Hinchley.

VII. The combination of Krishnamurthy, Adolph, and Boice.

The applicant argues that the combination of Krishnamurthy, Adolph, and Boice doses teach the claimed features as specified in claims 21, 22, 24, and 35.

The examiner respectfully disagrees with the applicant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above.

Boice teaches each of motion estimation processors (52 of fig. 4) comprises a plurality of search processors (see Abstract: a consequence of the multiple processors subdividing the extended window and analyzing each subdivision in parallel) that operate in parallel upon a single macroblock (figs. 1 and 3), and each search processor operating at a different one of a plurality of pixels blocks (scaling or half pixel search, quarter pixel search, 36, 38, and 40 of fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the plurality of search processors (52 of fig. 4) of Boice into each of motion estimation processor of Krishnamurthy and Adolph to provide the process of motion estimation effectively reduces the temporal redundancy in successive video frames by exploiting the temporal correlation (similarities) that often exists between successive frames.

VIII. The combination of Krishnamurthy, Adolph, Boice, and Kopet.

The applicant argues that the combination of Krishnamurthy, Adolph, and Boice doses teach the claimed features as specified in claims 21, 22, 24, and 35.

The examiner respectfully disagrees with the applicant. It is submitted that the combination of Krishnamurthy and Adolph teaches all limitations as described above.

Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29). Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Krishnamurthy Adolph,

and Boice in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung Vo whose telephone number is 571-272-7340. The examiner can normally be reached on Monday-Wednesday, Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Ustaris can be reached on 571-272-7383. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Tung Vo/
Primary Examiner, Art Unit 2483